NXP Semiconductors
User's Guide

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FRDM-KW41Z Freedom Development Board

1. Introduction

This guide describes the hardware for the FRDM-KW41Z Freedom development board. The FRDM-KW41Z Freedom development board is a small, low-power, and cost-effective evaluation and development board for application prototyping and demonstration of the KW41Z/31Z/21Z (KW41Z) family devices. These evaluation boards offer:

- Easy-to-use mass-storage-device mode flash programmer.
- Virtual serial port.
- Standard programming and run-control capabilities.

The KW41Z is an ultra low-power, highly integrated single-chip device that enables Bluetooth Low Energy (BLE), Generic FSK (at 250, 500 and 1000 kbps) or IEEE Standard 802.15.4 with Thread support for portable, extremely low-power embedded systems.

The KW41Z integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, up to 512 KB Flash and up to 128 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications.

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2. FRDM-KW41Z overview and description

The FRDM-KW41Z development board is an evaluation environment supporting NXP's KW41Z/31Z/21Z (KW41Z) Wireless MCUs. The KW41Z integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range (supporting a range of FSK/GFSK and O-QPSK modulations) and an ARM Cortex-M0+ MCU into a single package. NXP supports the KW41Z with tools and software that include hardware evaluation and development boards, software development IDE, applications, drivers, custom PHY usable with IEEE Std. 802.15.4 compatible MAC, BLE Link Layer, and enables the usage of the Bluetooth Low Energy protocol in the MBAN frequency range for proprietary applications. The FRDM-KW41Z development board consists of the KW41Z device with a 32 MHz reference oscillator crystal, RF circuitry (including antenna), 4-Mbit external serial flash, and supporting circuitry in the popular Freedom board form-factor. The board is a standalone PCB and supports application development with NXP's Bluetooth Low Energy, Generic FSK and IEEE Std. 802.15.4 protocol stacks including Thread.

2.1. Board features

Figure 1 is a high-level block diagram of the FRDM-KW41Z board features.

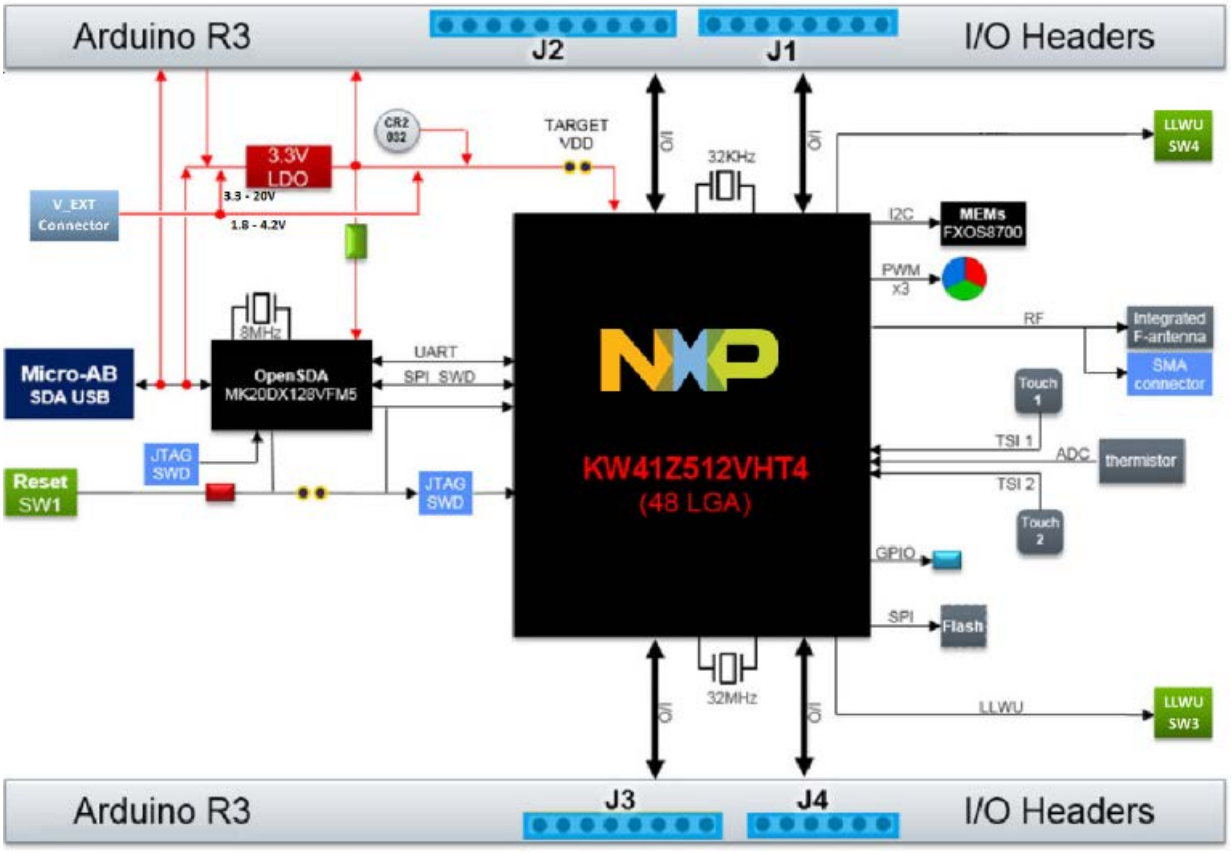

Figure 1. FRDM-KW41Z block diagram

2.1.1. FRDM-KW41Z board

The FRDM-KW41Z development board is based on NXP Freedom development platform. It is the most diverse reference design containing the KW41Z device and all necessary I/O connections for use as a stand-alone board, or connected to an application. The FRDM-KW41Z can also be used as an Arduino compatible shield. **Figure 2** shows the FRDM-KW41Z development board.

Figure 2. FRDM-KW41Z freedom development board

The FRDM KW41Z development board has these features:

- NXP's ultra-low-power KW41Z Wireless MCU supporting BLE, Generic FSK, and IEEE Std. 802.15.4 (Thread) platforms
- IEEE Std. 802.15.4, 2006-compliant transceiver supporting 250 kbps O-QPSK data in 5.0 MHz channels, and full spread-spectrum encoding and decoding
- Fully compliant Bluetooth v4.2 Low Energy (BLE)
- Reference design area with small-footprint, low-cost RF node:
  - Single-ended input/output port
  - Low count of external components
  - Programmable output power from -30 dBm to +3.5 dBm at the SMA connector, no harmonic trap, with DC/DC Bypass and Buck modes of operation

  - Receiver sensitivity is -100 dBm, typical (@1 % PER for 20-byte payload packet) for 802.15.4 applications, at the SMA connector
  - Receiver sensitivity is -95 dBm (for BLE applications).
- Integrated PCB inverted F-type antenna and SMA RF port
- Selectable power sources
- DC-DC converter with Buck, Boost, and Bypass operation modes
- 32 MHz reference oscillator
- 32 kHz reference oscillator
- 2.4 GHz frequency operation (ISM and MBAN)
- External serial flash memory for Over-the-Air Programming (OTAP) support
- Integrated Open-Standard Serial and Debug Adapter (OpenSDA)
- Cortex 10-pin (0.05″) SWD debug port for target MCU
- Cortex 10-pin (0.05″) JTAG port for OpenSDA updates
- One RGB LED indicator
- One red LED indicator
- Two push-button switches
- Two TSI buttons

Figure 3 shows the main board features and input/output headers for the FRDM-KW41Z board.

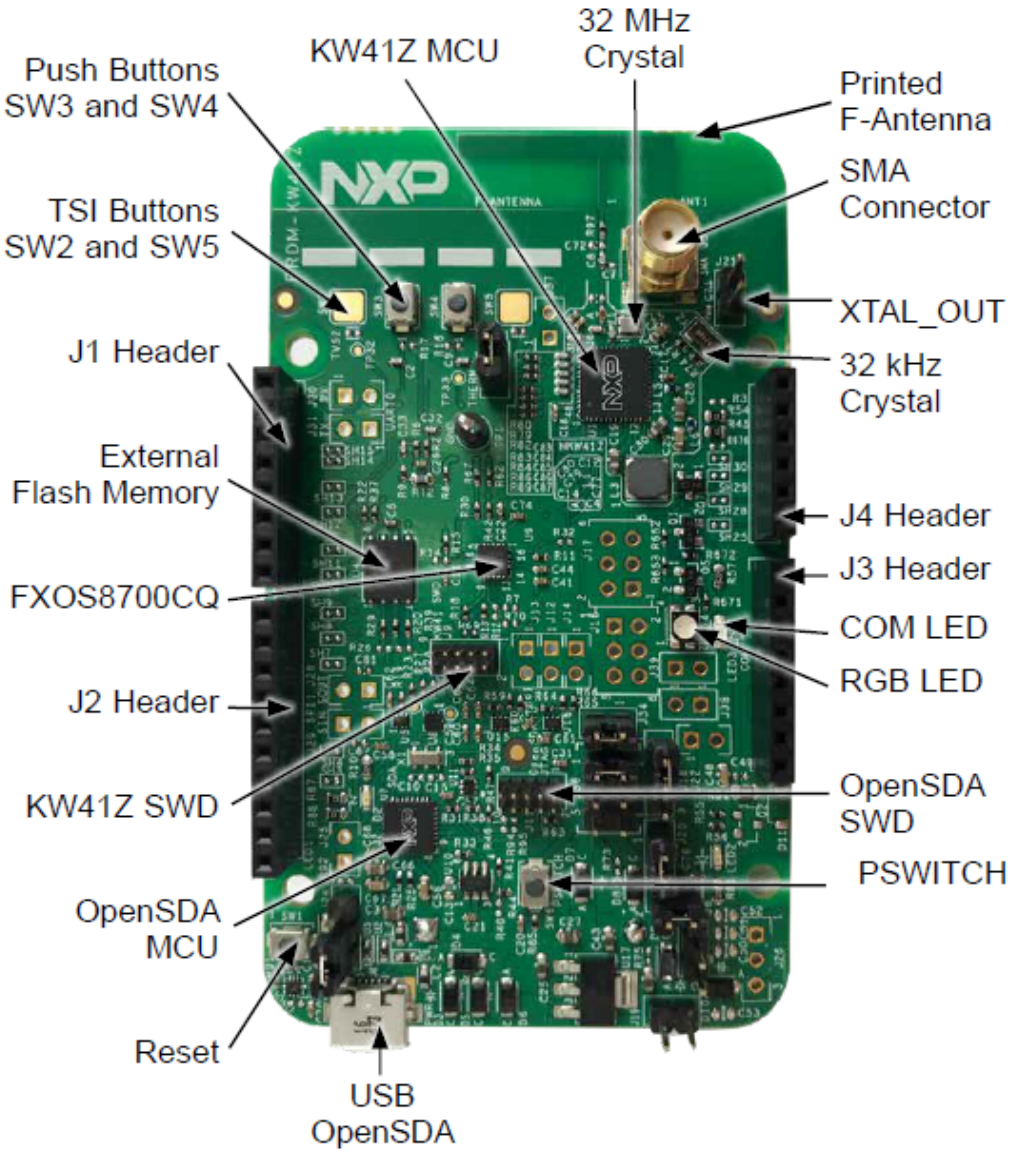

Figure 3. FRDM-KW41Z component placement

2.2. OpenSDA serial and debug

The FRDM-KW41Z development board includes OpenSDA v3.0-a serial and debug adapter circuit that includes an open-source hardware design, an open-source bootloader, and debug interface software. It bridges serial and debug communications between a USB host and an embedded target processor as shown in **Figure 4**. The hardware circuit is based on a NXP Kinetis K20 family microcontroller (MCU) with 128 KB of embedded flash and an integrated USB controller. OpenSDAv3.0 comes preloaded with the DAPLink bootloader - an open-source mass storage device (MSD) bootloader and the Segger J-Link Interface firmware, which provides a MSD flash programming interface, a virtual serial port interface, and a J-Link debug protocol interface. For more information on the OpenSDAv3.0 software, see mbed.org, https://github.com/mbedmicro/DAPLink, and https://www.segger.com/opensda.html.

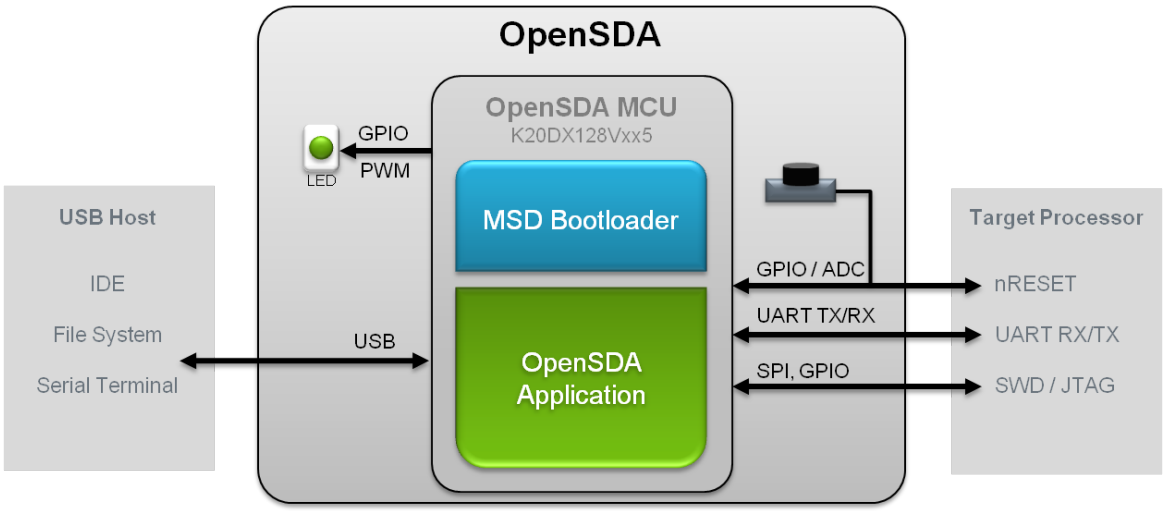

Figure 4. OpenSDAv3.0 high-level block diagram

OpenSDAv3.0 is managed by a Kinetis K20 MCU built on the ARM Cortex-M4 core. The OpenSDAv3.0 circuit includes a status LED (D2) and a pushbutton (SW1). The pushbutton asserts the Reset signal to the KW41Z target MCU. It can also be used to place the OpenSDAv3.0 circuit into bootloader mode. UART and GPIO signals provide an interface to either the SWD debug port or the K20. The OpenSDAv3.0 circuit receives power when the USB connector J6 is plugged into a USB host.

2.2.1. Virtual serial port

A serial port connection is available between the OpenSDAv3.0 MCU and pins PTC6 and PTC7 of the KW41Z.

NOTE

To enable the Virtual COM, Debug, and MSD features, Segger J-Link drivers must be installed. Download the drivers at https://www.segger.com/downloads/jlink.

3. Functional description

3.1. FRDM-KW41Z board overview

The FRDM-KW41Z board is built around NXP's KW41Z Wireless MCU in a 48-pin Laminate QFN package. It features an IEEE Std. 802.15.4 and BLE 2.4 GHz radio frequency transceiver and a Kinetis family ultra-low-power, mixed-signal ARM Cortex-M0+ MCU in a single package. This board is intended as a simple evaluation platform and as a building block for application development. The four-layer board provides the KW41Z with its required RF circuitry, 32 MHz reference oscillator crystal, and power supply with a DC-DC converter including Bypass, Buck, and Boost modes. The layout for this base-level functionality can be used as a reference layout for your target board.

Figure 5 shows the FRDM-KW41Z board with the location of the I/O headers. This list provides the details.

- J1, J2, J3, and J4:
  - Headers have standard 0.1 in (2.54) mm pin spacing
  - J2 is 10-pin
  - J1 and J3 are 8-pin
  - J4 is 6-pin
  - All pin headers mounted on the top side of the FRDM-KW41Z board are intended for plugging into matching receptacles on the NXP platform development board
- J38, J39, J16 and J18:
  - Headers have standard 0.1 in. (2.54 mm) pin spacing
  - J16, and J17 are 2 × 3 pins
  - J38 and J39 are 1 x 2 pins
  - Pin headers mounted on the top side of the FRDM-KW41Z are intended to select between power configurations, Bypass, Buck, and Boost.
  - Headers are not populated by default and shorting traces are used to select Buck mode out of the box.
- J36 and J34:
  - Has standard 0.1 in. (2.54 mm) pin spacing
  - 2 x 3 pin header for selecting the desired voltage source
  - J34 is a 2 x 1 pin header for measuring current into VDCDCIN
- J22 and J37
  - All headers have standard 0.1 in. (2.54 mm) pin spacing
  - Both headers are 1 x 2 headers and are meant for measuring current when V_BRD is used to power on-board peripherals and/or LEDs.
  - Both headers are not populated by default

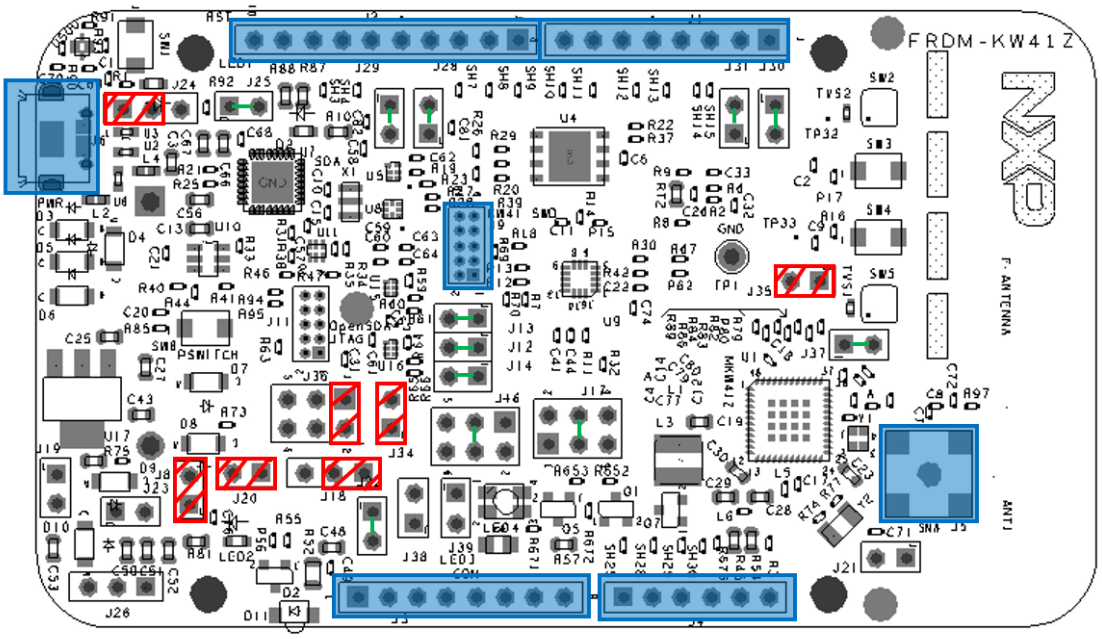

Figure 5. FRDM-KW41Z default jumper settings and key connectors

3.2. RF circuit

The KW41Z device includes an integrated transceiver includes a 1 mW nominal output power PA with internal Voltage-Controlled Oscillator (VCO), integrated transmit/receive switch, on-board power supply regulation, and full spread-spectrum encoding and decoding. The main specifications of the KW41Z are:

- Nominal output power is set to 0 dBm
- Programmable output power ranges from -30 dBm to +3.5 dBm at the SMA (no harmonic trap)
- Typical sensitivity is -100 dBm (@1 % PER for 25 °C) at the SMA (802.15.4)
- Typical sensitivity is -96 dBm (@1 % PER for 25 °C) at the SMA (BLE)
- Frequency ranges from 2360 to 2480 MHz
- Differential bidirectional RF input/output port with integrated transmit/receive switch

The FRDM-KW41Z RF circuit provides an RF interface for users to begin application development. A minimum matching network to the MCU antenna pin is provided through C4 and L1. An additional matching component, C, is provided to match the printed F-antenna to 50 ohm controlled line. The antenna circuit used in the FRDM-KW41Z design is shown in **Figure 6**.

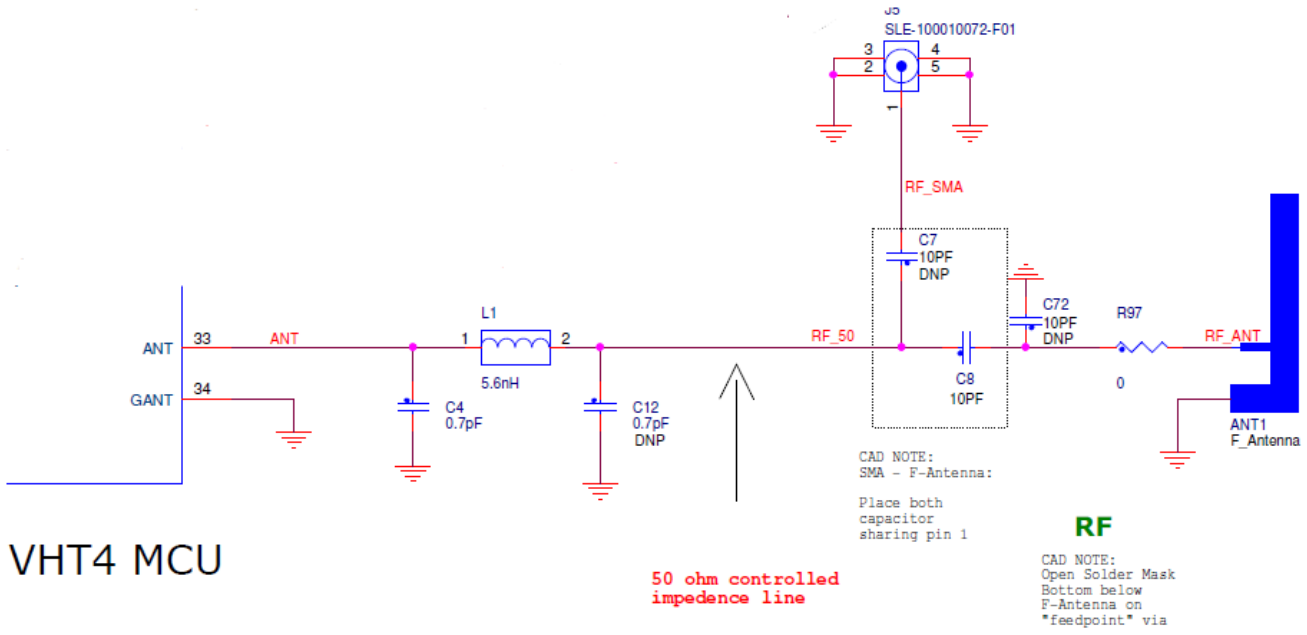

Figure 6. FRDM-KW41Z RF circuit

3.3. Clocks

The FRDM-KW41Z board provides two clocks: a 32 MHz clock for clocking the MCU and Radio, and a 32.768 kHz clock to provide an accurate low power time base.

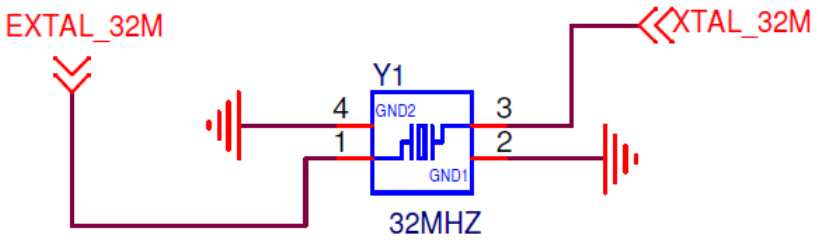

Figure 7. FRDM-KW41Z 32 MHz reference oscillator circuit

- 32 MHz Reference Oscillator
  - **Figure 7** shows the 32 MHz external crystal Y1. The IEEE Std. 802.15.4 requires the frequency to be accurate to less than ±40 ppm. The FRDM-KW41Z is equipped with a ±10 ppm oscillator.
  - Internal load capacitors provide the bulk of the crystal load capacitance.
  - To measure the 32 MHz oscillator frequency, program the CLKOUT (PTB0) signal to provide buffered output clock signal

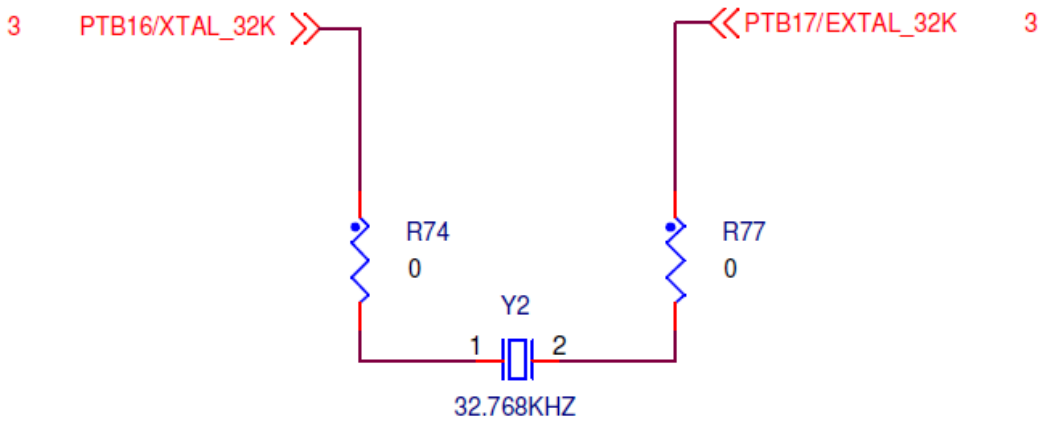

Figure 8. FRDM-KW41Z 32.786 kHz oscillator circuit

- 32.768 kHz Crystal Oscillator (for accurate low-power time base)
  - A secondary 32.768 kHz crystal Y2 is provided (see **Figure 8**)
  - Internal load capacitors provide the entire crystal load capacitance
  - Zero ohm resistors are supplied to bypass the Y2 crystal
    - This provides two extra GPIO to the I/O headers; PTB16 & PTB17

3.4. Power management

There are several ways to power and measure current on the FRDM-KW41Z board. The FRDM-KW41Z voltage selection and current measurement circuit is shown in **Figure 9**.

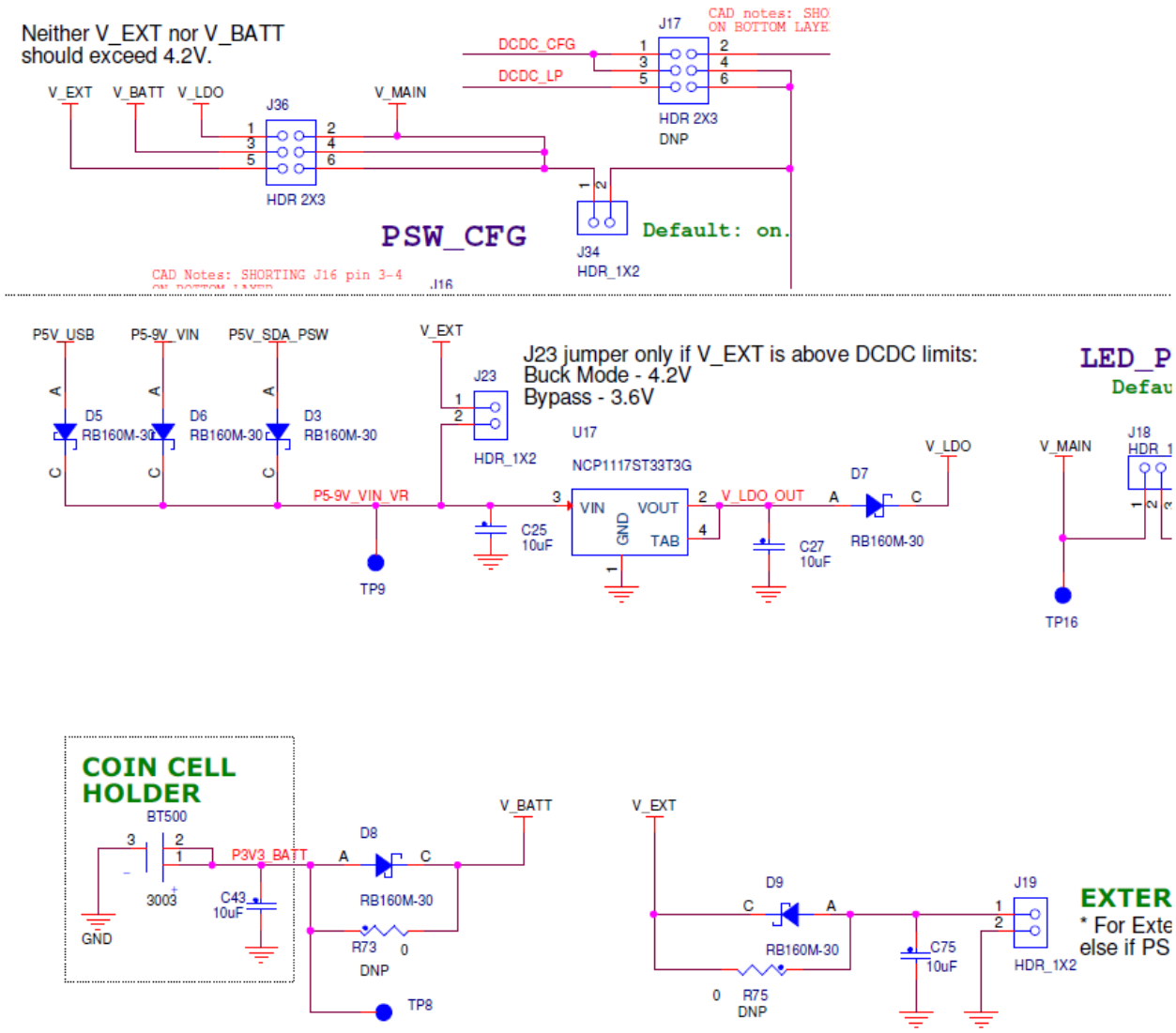

Figure 9. FRDM-KW41Z Voltage source and IDD measurement circuit

The FRDM-KW41Z can be powered by the following means:

- Through the micro USB type B connector (J6), which provides 5 V to the P5 V_USB signal into the LDO 3V3 (U17)
- Through the Freedom development board headers, which provide either P3.3 V or P5-9 V_VIN on header J3 pin-8 to LDO 3V3 (U17)
- From an external battery (Coin-cell – CR2032)
- From an external DC supply in the following ways
  - Connect an adapter that can supply 1.8 to 3.6 VDC to J19 pins, then connect V_MAIN to the V_EXT source using jumper J36 (connect pins 5 and 6).

– Connect an unregulated external supply (of up to 5.5 VDC) to J19 pins and then connect V_EXT to the source of the on board 3.3 V LDO regulator (using the selector J23 pin 1-2). Be sure to select V_LDO as the source for V_MAIN using jumper J36 (pins 1 and 2).

The 2-pin 1×2 headers J8 and J20 can supply current to various board components and can be used to measure the current of the board components (if desired). Green LED marked as LED2 is available as a power indicator.

Power headers can supply either the LED, MCU, or peripheral circuits. Measure the current by inserting a current meter in place of a designated jumper. See **Table 4** for details on jumper descriptions.

The FRDM-KW41Z can be configured to use any of the DCDC converter operating modes. These modes are Bypass, Buck (Manual-Start), Buck (Auto-Start), and Boost. **Figure 10** to **Figure 13** highlight the jumper settings for each of these modes.

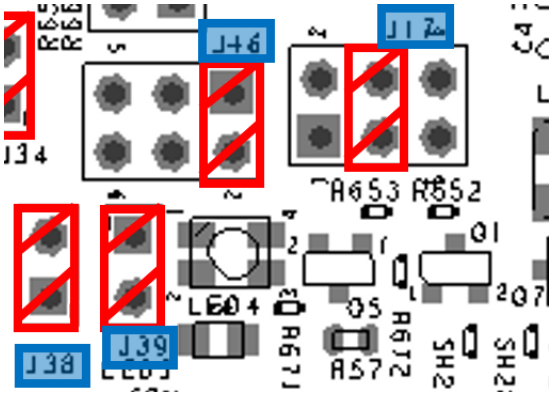

Figure 10. Jumper settings for Bypass mode

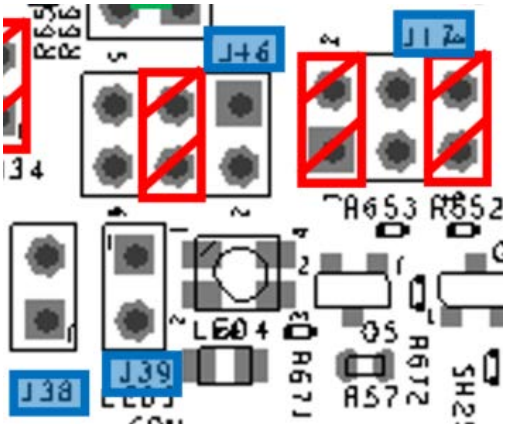

Figure 11. Jumper settings for Boost mode

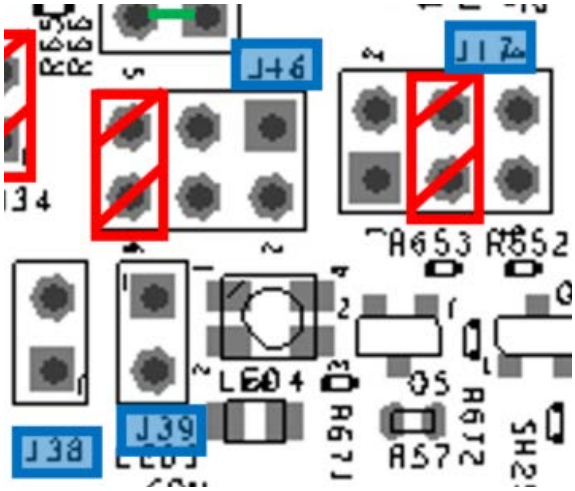

Figure 12. Jumper settings for Buck mode (Manual-start)

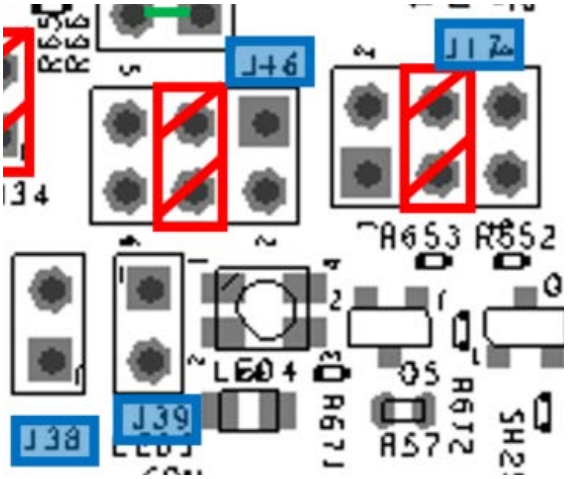

Figure 13. Jumper settings for Buck mode (Auto-start)

Table 1 describes DCDC mode jumper configurations.

Table 1. DCDC configurations

Mode	J16	J17	J38	J39
Bypass Mode	1-2	3-4	ON	ON
Boost Mode	3-4	1-2 5-6	OFF	OFF
Buck Mode (manual start)	5-6	3-4	OFF	OFF
Buck Mode (auto start)	3-4	3-4	OFF	OFF

4. FRDM-KW41Z board peripheral functions

The FRDM-KW41Z development board includes the Freedom development board headers to interface with the general-purpose functions, and to assist in the implementation of target applications. The FRDM-KW41Z board has alternate port functions routed to those interface headers to leverage the off-board Freedom development platform peripherals.

4.1. Serial flash memory

Component U4 is the AT45DB041E 4-Mbit (512 KB) serial flash memory with SPI interface. It is intended for Over-The-Air Programming (OTAP), or for storing the non-volatile system data or parameters.

Figure 14 shows the memory circuit.

- Memory power supply is P3V3_BRD
- Discrete pull-up resistors pads for SPI port
- You can share the SPI with other peripherals using the J1 I/O header
- The SPI Write Protect and Reset have a discrete pull-up resistor

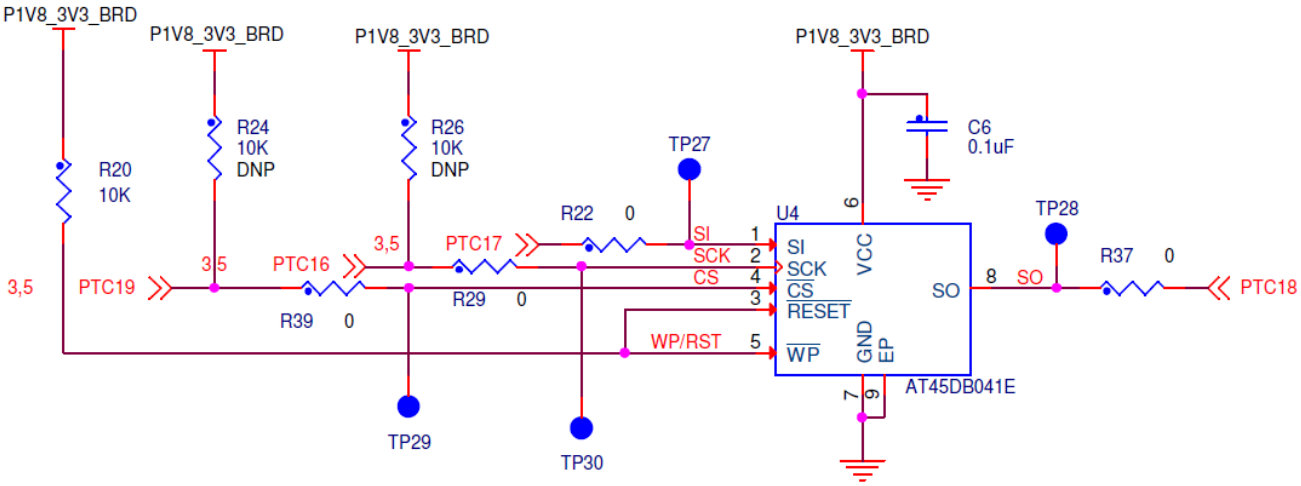

Figure 14. AT45DB041E 4-Mbit (512 KB) serial flash memory circuit

4.2. Accelerometer and magnetometer combo sensor

Component U9 is NXP FXOS8700CQ sensor, a six-axis sensor with integrated linear accelerometer and magnetometer, very low power consumption, and selectable I^2C interface. **Figure 15** shows the sensor circuit.

- The sensor power supply is P1V8_3V3_BRD
- Discrete pull-up resistors for the I^2C bus lines are provided
- Default address is configured as 0x1F:
- Address can be changed by pull-up/pull-down resistors on SA0 and SA1 lines
- There is one interrupt signal routed
- The I^2C can be shared with other peripherals through the J4 I/O header

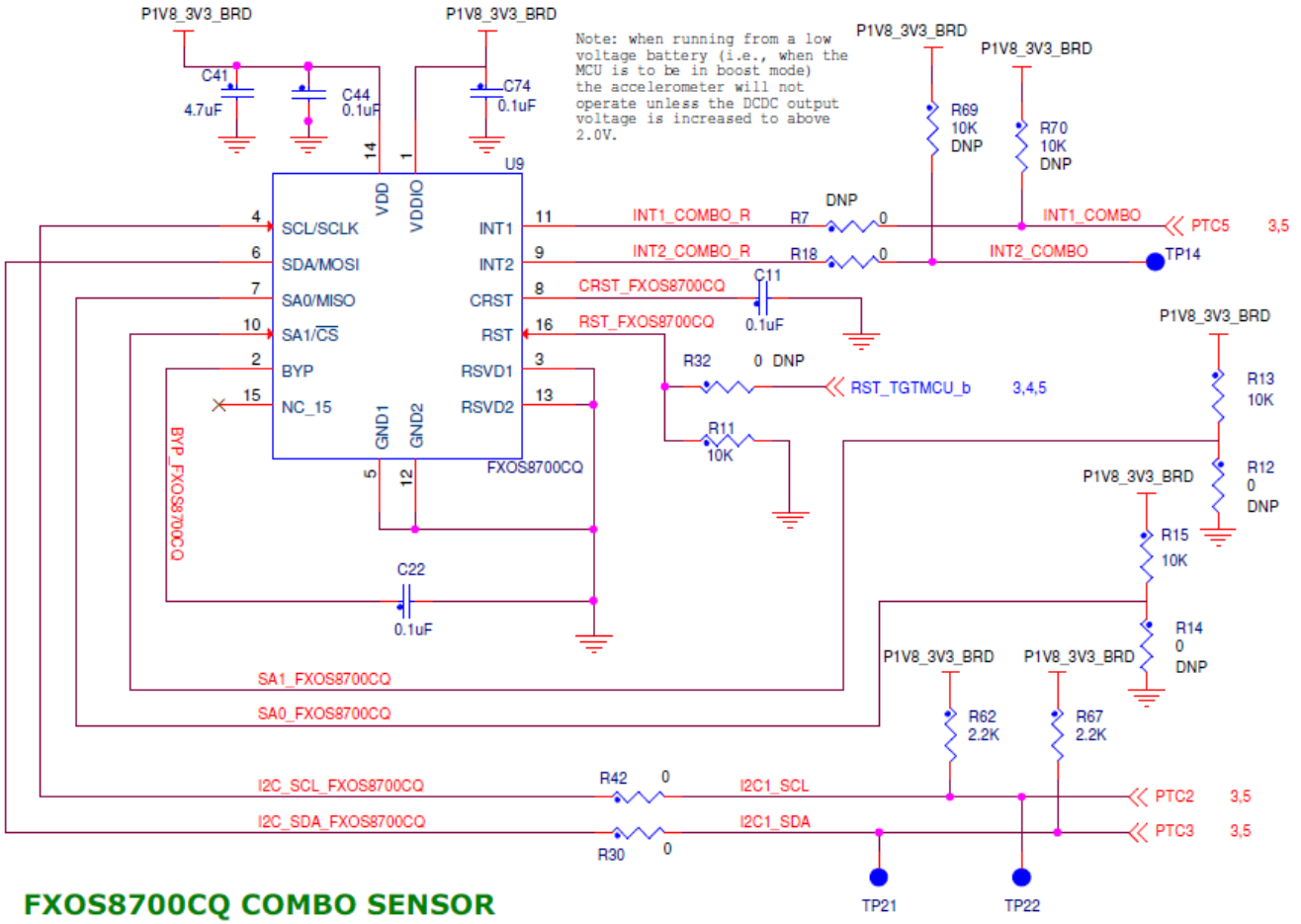

Figure 15. FXOS8700CQ combo sensor circuit

4.3. Thermistor

One thermistor (RT2) is connected to two ADC inputs (ADC0_DP0 & ADC_DM0) of KW41Z for evaluating the ADC module, as shown in **Figure 16**.

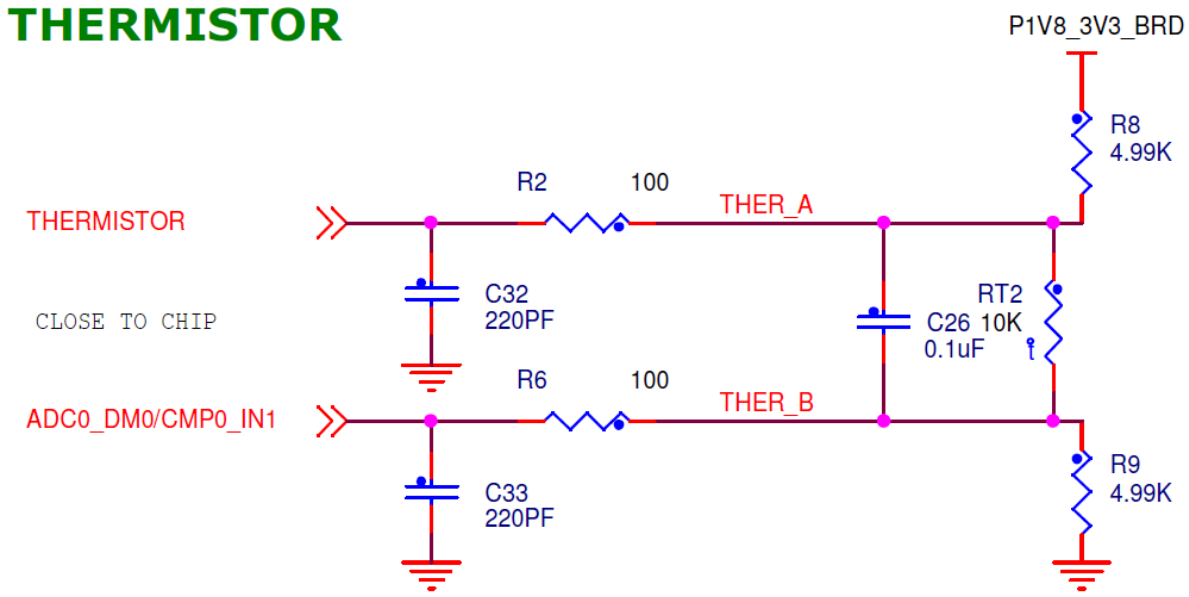

Figure 16. Thermistor circuit

The high side of the Thermistor circuit is attached to ADC0_DP0 through J35. See **Figure 17** for details.

Figure 17. ADC0_DP0 selection jumper

4.4. User application LEDs

The FRDM-KW41Z provides a RGB LED and a single Red LED for user applications. **Figure 18** and **Figure 19** show the circuitry for the application controlled LEDs.

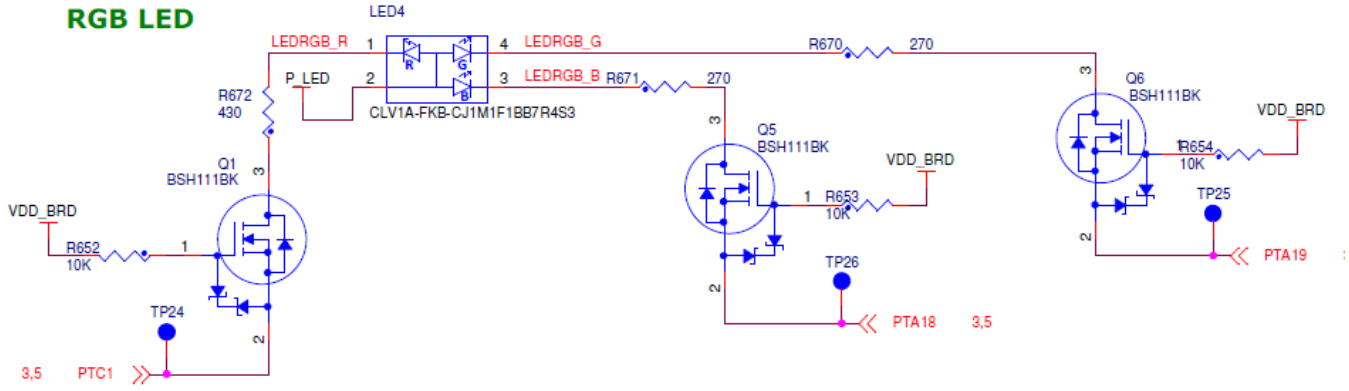

Figure 18. FRDM-KW41Z RBD LED circuit

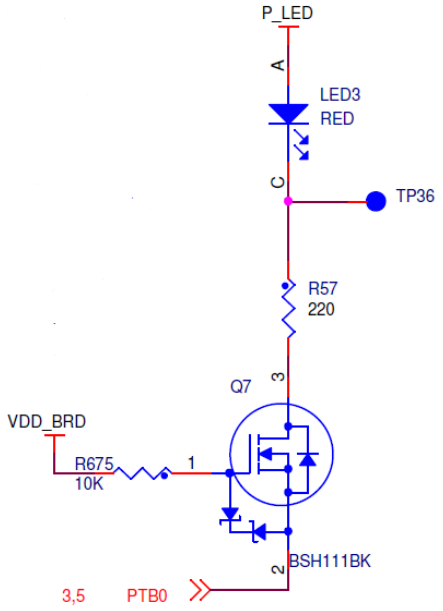

Figure 19. FRDM-KW41Z communicating LED circuit

The user application LED circuitry is designed to operate when V_BRD is at 3.3V or 1.8V. P_LED must be greater than 2.7 V to operate all the LEDs. Jumper J18 allows the selection of different voltages for P_LED.

- When operating in Buck mode, J18 jumper selector should select pins 1-2.
- When operating in Boost mode, J18 jumper selector should select pins 2-3.
- Bypass mode can use either selection.

When pins 2-3 are selected, the LED current will be included in the MCU IDD if measured from jumper J34. Therefore, jumper footprints J22 and J37 were included in the design. If you need to measure the MCU IDD and have these LEDs operating at VDD_BRD levels, then you can install a 2-pin jumper in J22 and J37 to measure the MCU current (remember to cut the cut trace on the bottom of the board for these jumpers).

4.5. Buttons and electrodes

Two tactile buttons and two TSI electrodes are populated on the FRDM-KW41Z for Human Machine Interaction (HMI). **Figure 20** shows the circuit for both the TSI electrodes and the tactile buttons.

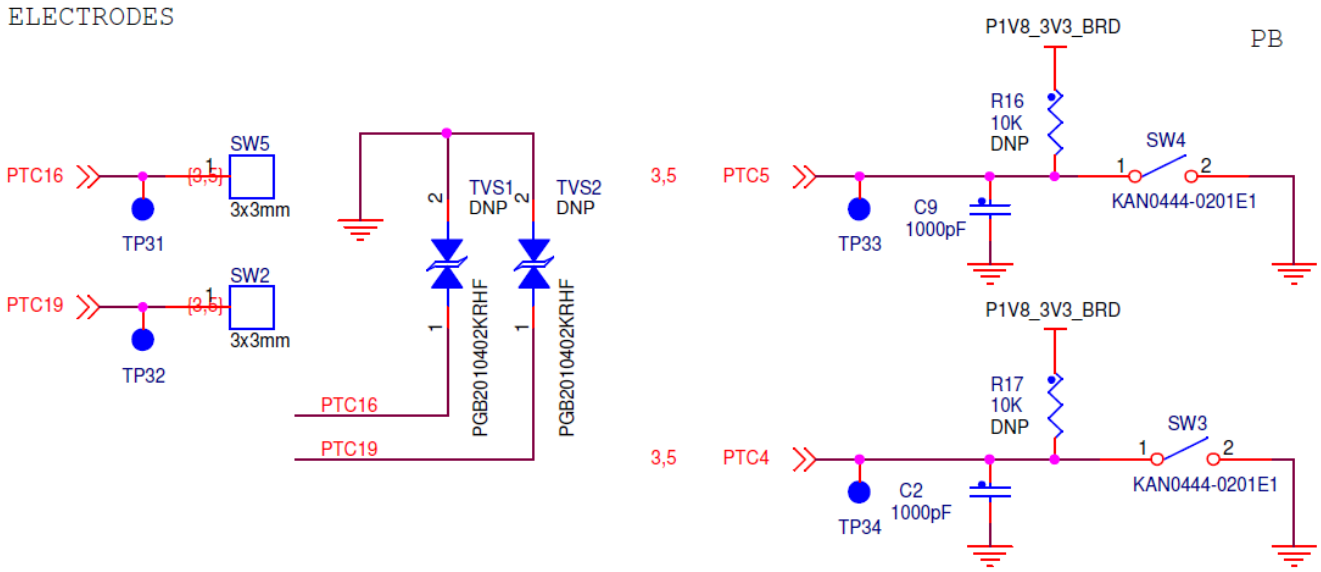

Figure 20. FRDM-KW41Z HMI circuit

4.6. IR transmitter

An infrared transmitter or blaster is provided to communicate over infra-red via the CMT module on the KW41Z.

Figure 21 shows the IR circuit.

- The IR power supply is P3V3_LED.
- The IR has a range of approximately 10 meters.
- The current draw is approximately 100 mA when active.

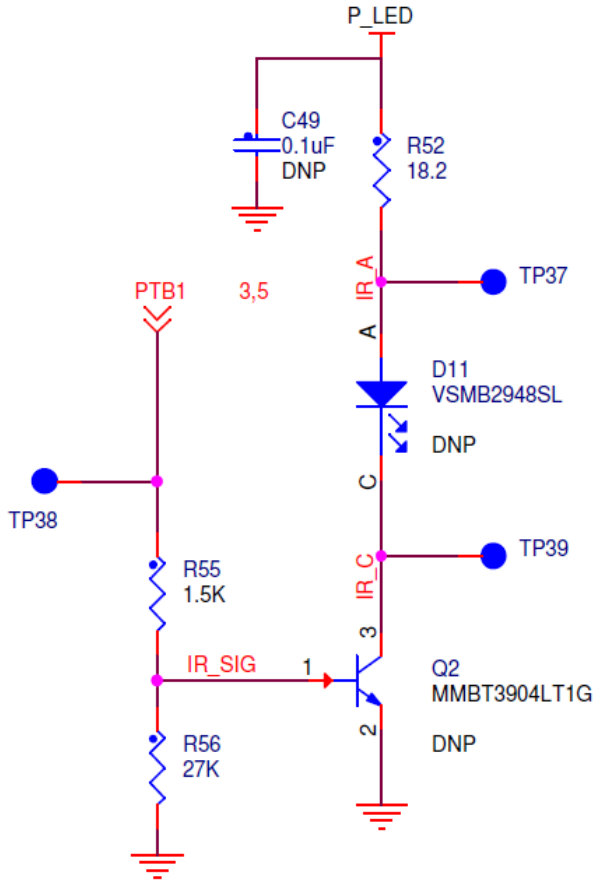

Figure 21. IR transmitter circuit

NOTE

Components D11 and Q2 are not populated by default. They must be populated for the IR transmitter circuit to function.

4.7. Interface connectors J1, J2, J3, and J4

Figure 22 shows the I/O pinout.

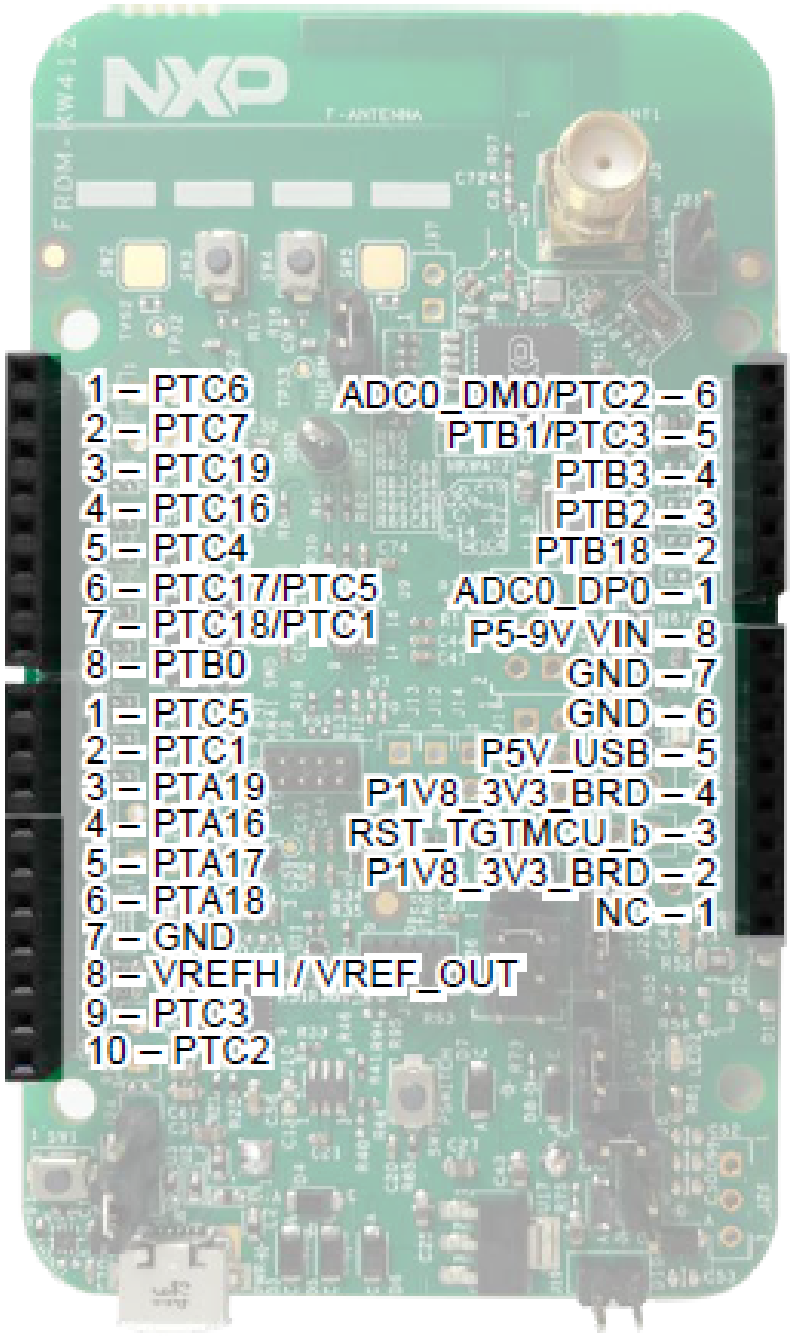

Figure 22. FRDM-KW41Z I/O header pinout

Table 2. Arduino compatible header/connector pinout (J1 and J2)

HDR pin	1x10 Connector (J2) - Description	IC pin
1	PTC5/TSI0_CH1/LLWU_P13/RF_NOT_ALLOWED/LPTMR0_ALT2/LPUART0_RTS_b/TPM1_CH1/BSM_CLK	41
2	PTC1/ANT_B/I2C0_SDA/LPUART0_RTS_b/TPM0_CH2/BLE_RF_ACTIVE	37
3	PTA19/TSI0_CH13/ADC0_SE5/LLWU_P7/SPI1_PCS0/TPM2_CH1	7
4	PTA16/TSI0_CH10/LLWU_P4/SPI1_SOUT/TPM0_CH0	4
5	PTA17/TSI0_CH11LLWU_P5/RF_RESET/SPI1_SIN/TPM_CLKIN1/DTEST5/dcdc_testo3	5
6	PTA18/TSI0_CH12/LLWU_P6/SPI1_SCK/TPM_CH0/DTEST6/dcdc_testo4	6
7	GND	
8	VREFH/VREF_OUT	27
9	PTC3/TSI0_CH15/DIAG2/LLWU_P11/RX_SWITCH/I2C1_SDA/UART0_TX/TPM0_CH1/DTEST7/DTM_TX	39
10	PTC2/TSI0_CH14/DIAG1/LLWU_P10/TX_SWITCH/I2C1_SCL/UART0_RX/CMT_IRO/DTEST6/DTM_RX	38
HDR pin	**1x8 Connector (J1) - Description**	**IC pin**
1	PTC6/TSI0_CH2/LLWU_14/XTAL_OUT_EN/I2C1_SCL/UART0_RX/TPM2_CH0/DTEST2/BSM_FRAME	42
2	PTC7/TSI0_CH3/LLWU_P15/SPI0_PCS2/I2C1_SDA/UART0_TX/TPM2_CH1/DTEST3/BSM_DATA	43
3	PTC19/TSI0_CH7/LLWU_P3/SPI0_PCS0/I2C0_SCL/UART0_CTS_b/BSM_CLK/DTEST3/RF_ACTIVE	48
4	PTC16/TSI0_CH4/LLWU_P0/SPI0_SCK/I2C0_SDA/UART0_RTS_b/TPM0_CH3/DTEST0/dcdc_testo1	45
5	PTC4/TSI0_CH0/DIAG3/LLWU_P12/ANT_A/EXTRG_IN/UART0_CTS_b/TPM1_CH0/DTEST0/BSM_DATA	40
6A	PTC17/TSI0_CH5/LLWU_P1/SPI0_SOUT/I2C1_SCL/UART0_RX/BSM_FRAME/DTEST1/DTM_RX	46
6B	PTC5/TSI0_CH1/LLWU_P13/RF_NOT_ALLOWED/LPTMR0_ALT2/LPUART0_RTS_b/TPM1_CH1/BSM_CLK	41
7A	PTC18/TSI0_CH6/LLWU_P2/SPI0_IN/I2C1_SDA/UART0_TX/BSM_DATA/DTEST2/DTM_TX	47
7B	PTC1/ANT_B/I2C0_SDA/LPUART0_RTS_b/TPM0_CH2/BLE_RF_ACTIVE	37
8	PTA19/TSI0_CH13/ADC0_SE5/LLWU_P7/SPI1_PSC0/TPM2_CH1	7

Table 3. Arduino compatible header/connector pinout (J3 and J4)

HDR Pin	1x8 Connector (J3) - Description	IC Pin
1	NC	
2	IOREF(3V3)	
3	PTA2/TPM0_CH3/RESET_b	3
4	3V3	
5	5V	
6	GND	
7	GND	
8	5-9V IN	
HDR Pin	**1x6 Connector (J4) - Description**	**IC Pin**
1	ADC0_DP0/CMP0_IN0	24
2	DAC0_OUT/ADC0_SE4/CMP0_IN2	23
3	ADC0_SE3/CMP0_IN3	18
4	ADC0_SE2/CMP0_IN4	19
5A	ADC0_SE1/CMP0_IN5	17
5B	PTC3/TSI0_CH15/LLWU_P11/RX_SWITCH/I2C1_SDA/UART0_TX	39
6A	ADC0_DM0/CMP0_IN1	25
6B	PTC2/TSI0_CH14/LLWU_P10/TX_SWITCH/I2C1_SCL/LPUART0_RX/CMT_IRO/DTM_RX	38

5. Jumper table

Table 4. FRDM-KW41Z jumper table

Jumper	Option	Setting	Description
J8[1]	P3V3_BRD	**1-2**	Isolate board supply to board peripherals
J12	SWD_CLK_TGTMCU	**1-2***[2]	Isolate SWD_CLK from SWD header
J13	SWD_DIO	**1-2***	OpenSDA SWD_DIO isolation jumper
J14	SWD_CLK	**1-2***	OpenSDA SWD_CLK isolation jumper
J16	PSW_CFG	1-2 **3-4*** 5-6	PSWITCH to ground PSWITCH to VDCDC_IN PSWITCH to SW6
J17	DCDC_CFG	**3-4*** 1-2; 5-6	**DCDC_CFG to VDCDC_IN** DCDC_CFG to ground; DCDC_LP to VDCDC__IN
J18	PWR_CFG	**1-2** 2-4	**V_MAIN to P_LED and P_LED_PWR** VDD_BRD to P_LED and P_LED_PWER
J19	External PS	1-2	Allows for an external power supply to be connected.
J20	P_LED	**1-2**	**Isolate board power LED supply**
J21	XTAL_OUT_CON	1-2	Allows for XTAL_OUT signal to be connected to other devices that may require synchronization with the RF clock.
J22	VDD_MCU	**1-2***	Isolate MCU 1P8 power supply
J23	V_EXT	1-2	Connect external supply to VIN of U17 (regulator)
J24	RST Button Bypass	**1-2** 2-3	**Reset button connected to OpenSDA** Reset button connected to Target MCU
J25	SDA_RST_TGTMCU	**1-2***	**Isolate OpenSDA MCU from target MCU reset signal**
J28/J29	SPI IN/OUT	**J28-1 J28-22 / J29-1 J29-2** J28-1 J29-2 / J28-2 J29-1	**SOUT to J2-4 / SIN to J2-5** SOUT to J2-5 / SIN to J2-4
J30/J31	UART RX/TX	**J30-1 J30-2 / J31-1 J31-2** J30-1 J31-2 / J30-2 J31-1	**RX to J1-1 / TX to J1-2** RX to J1-2 / TX to J1-1
J34	**VDCDC_IN**	**1-2**	**Isolate VDCDC_IN from V_MAIN**
J35	ADC SELECTOR	1-2	Isolate ADC0_DP0 from THERMISTOR
J36	**V_MAIN**	**1-2** 3-4 5-6	**Select V_LDO as the source for V_MAIN** Select V_BATT as the source for V_MAIN Select V_EXT as the source for V_MAIN
J37	**VDD_RF**	**1-2***	**Isolate VDD_RF**
J38	**VDD_MCU**	1-2	Connect VDCDC_IN to VDD_MCU (for bypass mode ONLY)
J39	VDD_RF	1-2	Connect VDCDC_IN to VDD_RF (for bypass mode ONLY)

1. Bold text indicates default selection.
2. *Denotes jumper selection is shorted on board.

6. References

The following references are available on www.nxp.com/FRDM-KW41Z:

- FRDM-KW41Z Design Package

7. Revision history

Table 5. Revision history

Revision number	Date	Substantive changes
0	07/2016	Initial release
1	04/2018	Modified to support FRDM-KW41Z rev C2

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